WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device comprising:

a first semiconductor substrate, in which, a memory cell array including a plurality of nonvolatile semiconductor memory cells, a plurality of bit lines electrically connected to the memory cell array, a plurality of word lines electrically connected to the memory cell array, a plurality of input terminals, and a plurality of transfer gate transistors each having one end electrically connected to a corresponding one of the word lines and another end electrically connected to a corresponding to one of the input terminals, are provided; and

a second semiconductor substrate, in which, a plurality of output terminals electrically connected to the input terminals of the first semiconductor substrate, and a word line control circuit configured to control the word lines and electrically connected to the output terminals, are provided.

2. The device according to claim 1, wherein the second semiconductor substrate stacked on the first semiconductor substrate.

3. The device according to claim 1, further comprising:

a plurality of first semiconductor substrates, wherein the second semiconductor substrate stacked on

at least one of the plurality of first semiconductor substrates.

4. The device according to claim 1, further comprising:

a first package which seals the first semiconductor substrate, the first package having a plurality of first terminals electrically connected to the input terminals of the first semiconductor substrate, the first terminals being provided on a side surface of the first package;

a second package which seals the second semiconductor substrate, the second package having a plurality of second terminals electrically connected to the output terminals of the second semiconductor substrate, the second terminals being provided on a side surface of the second package; and

a plurality of wirings which electrically connects the first terminals of the first package and the second terminals of the second package, the wirings being provided on the side surfaces of the first package and the second package.

5. The device according to claim 4, wherein the second package stacked on a surface different from the side surface of the first package.

6. The device according to claim 4, further comprising:

a plurality of first packages,

wherein the second package stacked on a surface different from the side surface of at least one of the first packages.

7. The device according to claim 4, further comprising:

a third package which seals the first package, the second package and the wirings.

8. The device according to claim 6, further comprising:

a third package which seals the first packages, the second package and the wirings.

9. A semiconductor integrated circuit device comprising:

a first semiconductor substrate, in which, a memory cell array including a plurality of nonvolatile semiconductor memory cells, a plurality of bit lines electrically connected to the memory cell array, a plurality of word lines electrically connected to the memory cell array, a plurality of input terminals, and a plurality of transfer gate transistors each having one end electrically connected to a corresponding one of the word lines and another end electrically connected to a corresponding to one of the input terminals, are provided; and

a second semiconductor substrate, in which, a plurality of output terminals electrically connected to the input terminals of the first semiconductor

substrate, and a word line control circuit configured to control the word lines and electrically connected to the output terminals, an interface circuit, and a plurality of interface terminals electrically connected to the interface circuit, are provided.

10. The device according to claim 9, further comprising:

a first package which seals the first semiconductor substrate, the first package having a plurality of first terminals electrically connected to the input terminals of the first semiconductor substrate, the first terminals being provided on a side surface of the first package;

a second package which seals the second semiconductor substrate, the second package having a plurality of second terminals electrically connected to the output terminals of the second semiconductor substrate, and a plurality of third terminals electrically connected to the interface terminals of the second semiconductor substrate, the second terminals being provided on a side surface of the second package and the third terminals being provided on a surface of the second package opposite to a lamination surface with the first package; and

a plurality of wirings which electrically connects the first terminals of the first package and the second terminals of the second package, the wirings being

provided on the side surfaces of the first package and the second package.

11. The device according to claim 10, wherein the second package stacked on a surface different from the side surface of the first package.

12. The device according to claim 10, further comprising:

a plurality of first packages,

wherein the second package stacked on a surface different from the side surface of at least one of the first packages.

13. The device according to claim 10, further comprising:

a third package which seals the first package, the second package and the wiring, the third package having a plurality of fourth terminals electrically connected to the third terminals of the second package.

14. The device according to claim 12, further comprising:

a third package which seals the first packages, the second package and the wirings, the third package having a plurality of fourth terminals electrically connected to the third terminals of the second package.

15. A semiconductor integrated circuit device comprising:

a first semiconductor substrate, in which, a memory cell array including a plurality of nonvolatile

semiconductor memory cells, a plurality of bit lines electrically connected to the memory cell array, a first shift register configured to control the bit lines, a plurality of word lines electrically connected to the memory cell array, a plurality of input terminals, a plurality of transfer gate transistors each having one end electrically connected to a corresponding one of the word lines and another end electrically connected to a corresponding to one of the input terminals, and a second shift register configured to control the transfer gate transistors, are provided; and

a second semiconductor substrate, in which, a plurality of output terminals electrically connected to the input terminals of the first semiconductor substrate, and a word line control circuit configured to control the word lines and electrically connected to the output terminals, are provided.

16. The device according to claim 15, wherein the second semiconductor substrate stacked on the first semiconductor substrate.

17. The device according to claim 15, further comprising:

a plurality of first semiconductor substrates, wherein the second semiconductor substrate stacked on at least one of the plurality of first semiconductor substrates.

18. The device according to claim 15, wherein the second semiconductor substrate, in which, a storage circuit which stores an address of a defected memory cell in the memory cell array, is provided.

19. A nonvolatile semiconductor memory system comprising:

a memory having a memory cell array including a plurality of nonvolatile semiconductor memory cells;

a control portion configured to control the memory;

a network interface connectable to a network;

a file management portion connected to the network interface configured to manages a relation between a data file given from the network and an address of the memory cell array; and

a memory interface connected to the file management portion configured to convert a signal given from the network to a signal which capable of used at the control portion.

20. The system according to claim 19, wherein the network interface corresponds to a transmission control protocol/internet protocol.

21. The system according to claim 20, wherein the network interface connectable to the network by using a file transfer protocol.

22. The system according to claim 20, wherein the network interface connectable to the network by using

an anonymous file transfer protocol.

23. The system according to claim 20, wherein the network interface connectable to the network by using a point-to-point protocol.

24. A nonvolatile semiconductor memory device comprising:

a first semiconductor substrate, in which, a memory having a memory cell array including a plurality of nonvolatile semiconductor memory cells, is provided; and

a second semiconductor substrate, in which, a control portion configured to control the memory, a network interface connectable to a network, a file management portion connected to the network interface configured to manages a relation between a data file given from the network and an address of the memory cell array, and a memory interface connected to the file management portion configured to convert a signal given from the network to a signal which capable of used at the control portion, are provided.

25. The device according to claim 24, wherein the second semiconductor substrate stacked on the first semiconductor substrate.

26. The device according to claim 24, further comprising:

a plurality of first semiconductor substrates, wherein the second semiconductor substrate stacked on

at least one of the plurality of first semiconductor substrates.

27. The device according to claim 24, further comprising:

a first package which seals the first semiconductor substrate, the first package having a plurality of first terminals electrically connected to the memory cell array, the first terminals being provided on a side surface of the first package;

a second package which seals the second semiconductor substrate, the second package having a plurality of second terminals electrically connected to the memory interface, and a plurality of third terminals electrically connected to the network interface, the second terminals being provided on a side surface of the second package and the third terminals being provided on a surface of the second package opposite to a lamination surface with the first package;

a plurality of wirings which electrically connects the first terminals of the first package and the second terminals of the second package, the wirings being provided on the side surfaces of the first package and the second package.

28. The device according to claim 27, wherein the second package stacked on a surface different from the side surface of the first package.

29. The device according to claim 27, further comprising:

a plurality of first packages,

wherein the second package stacked on a surface different from the side surface of at least one of the first packages.

30. The device according to claim 27, further comprising:

a third package which seals the first package, the second package and the wiring, the third package having a plurality of fourth terminals electrically connected to the third terminals of the second package.

31. The device according to claim 29, further comprising:

a third package which seals the first packages, the second package and the wirings, the third package having a plurality of fourth terminals electrically connected to the third terminals of the second package.